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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,771	04/03/2000	John R. McVey	10991816-1	4745

22879 7590 11/04/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

LAMB, TWYLER MARIE

ART UNIT	PAPER NUMBER
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2622

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/541,771	Applicant(s) MCVEY ET AL.	
	Examiner Twyler M. Lamb	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-9 and 11-34 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-21 is/are allowed.
- 6) ☒ Claim(s) 2-9, 11-12, 22-34 is/are rejected.
- 7) ☐ Claim(s) 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-6 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Farmwald et al. (Farmwald) (US 6,032,214).

With regard to claims and 11, Farmwald discloses a method for performing a transaction on a bus, comprising: receiving a signal requesting the transaction (col 6, line 52 – col 7, line 5); generating a first value using the signal (col 9, lines 21-36); storing the first value in a storage device (col 9, lines 21-36), with the first value including a plurality of bits indicating a beginning of usage of the bus (col 9, lines 21-36) and an ending of the usage of the bus for the transaction in terms of clock cycles (col 9, lines 21-36; col 12, line 56- col 13, line 3); and executing the transaction according to the first value (col 9, lines 21-36); storing the first value in the storage device includes storing the plurality of bits in storage elements included in the storage device, with those of the plurality of bits in a first state indicating the clock cycles during which the usage of the bus occurs for the transaction (col 9, lines 21-36).

With regard to claim 3, Farmwald also discloses each of the storage elements stores one of the plurality of bits (col 9, lines 21-36).

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With regard to claim 4, Farmwald also discloses receiving the signal includes receiving a second value indicating a number of the clock cycles during which the usage of the bus occurs for the transaction (col 12, line 56- col 13, line 3); generating the first value includes generating the plurality of bits using the second value with positions within the first value of those of the plurality of bits in the first state indicating the clock cycles during which the usage of the bus occurs for the transaction (col 12, line 56- col 13, line 3); and each of the positions within the first value corresponds to one of the storage elements (col 9, lines 21-36).

With regard to claim 5, Farmwald also discloses changing the first value in the storage device after storing in the first value and after an occurrence of at least one of the clock cycles by shifting ones of the plurality of bits between the storage elements (col 15, lines 6-23).

With regard to claim 6, Farmwald also discloses executing the transaction includes monitoring a first one of the positions to determine a beginning of the transaction (col 9, lines 21-36).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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4. Claims 7-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farmwald et al. (Farmwald) (US 6,032,214) in view of Sarangdhar et al. (Sarangdhar) (US 5,581,782).

With regard to claims 7 and 12, Farmwald differs from claim 7 in that he does not teach those of the plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition; and generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction.

Sarangdhar discloses a system that includes those of the plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition (col 2, line 63 – col 3, line 17); and generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction (col 2, line 63 – col 3, line 17).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Farmwald to include those of the plurality of bits in a second state indicate the clock cycles during which the bus exists in an idle condition; and generating the first value includes generating the plurality of bits in the second state so that the bus exists in the idle condition for at least one of the clock cycles between the usage of the bus for the transaction and the usage of the bus for a previous transaction as taught by Sarangdhar. It would have been obvious to one of ordinary

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skill in the art at the time of the invention to have modified Farmwald by the teaching of Sarangdhar to provide high performance symmetric arbitration protocol that includes support for priority agents and distributed arbitration by indicating which agent is busy or idle as taught by Sarangdhar in col 2, lines 37-46.

With regard to claim 8, Farmwald as modified also discloses the bus including a data bus (col 4, lines 13-15); the transaction includes an access to a memory device including a control phase and a data phase (col 7, lines 1-4); executing the transaction includes beginning the control phase when the first one of the positions enters the second state (col 7, lines 1-47); and executing the transaction includes beginning the data phase when a second one of the positions enters the first state (col 7, lines 1-47).

With regard to claim 9, Farmwald as modified also discloses the bus including an address bus (col 5, lines 16-28); the transaction includes an access to a memory device including a control phase (col 5, lines 16-28); executing the transaction includes beginning the control phase when the first one of the positions enters the first state (col 5, lines 16-28).

The limitations of claims 22-34 are met by the rejections above.

Allowable Subject Matter

5. Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. Claims 16-21 are allowed.

Response to Arguments

7. Applicant's arguments filed 4/7/04 have been fully considered but they are not persuasive.

8. Applicant argues that Farmwald does not anticipate every element as claimed in claims 2 and 11.

The Applicants argues that he can discern no teaching of "those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus Occurs" (from the amended claim 2) or "with positions within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus (from the amended claim 11) in Farmwald.

Farmwald discloses a bus transaction by sending a request packet (a sequence of bytes comprising address and control information) to one or more slave devices on the bus. An address can consist of 16 to 40 or more bits according to the teachings of this invention. Each slave on the bus must decode the request packet to see if that slave needs to respond to the packet. The slave that the packet is directed to must then begin any internal processes needed to carry out the requested bus transaction at the requested time. The requesting master may also need to transact certain internal processes before the bus transaction begins. After a specified access time the slave(s) respond by returning one or more bytes (8 bits) of data or by storing information made available from the

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bus. More than one access time can be provided to allow different types of responses to occur at different times in col 6, line 52 – col 7, line 15. This clearly reads on those of the plurality of bits in a first state corresponding to clock cycles during which the usage of the bus Occurs" (from the amended claim 2) or "with positions within the second value of those of the first plurality of bits in a first state corresponding to clock cycles during which the first data exists on the bus (from the amended claim 11).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Twyler M. Lamb whose telephone number is 703-308-8823. The examiner can normally be reached on M-Thurs 6:30-5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward L. Coles can be reached on 703-305-4712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Twyler M. Lamb
Primary Examiner
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